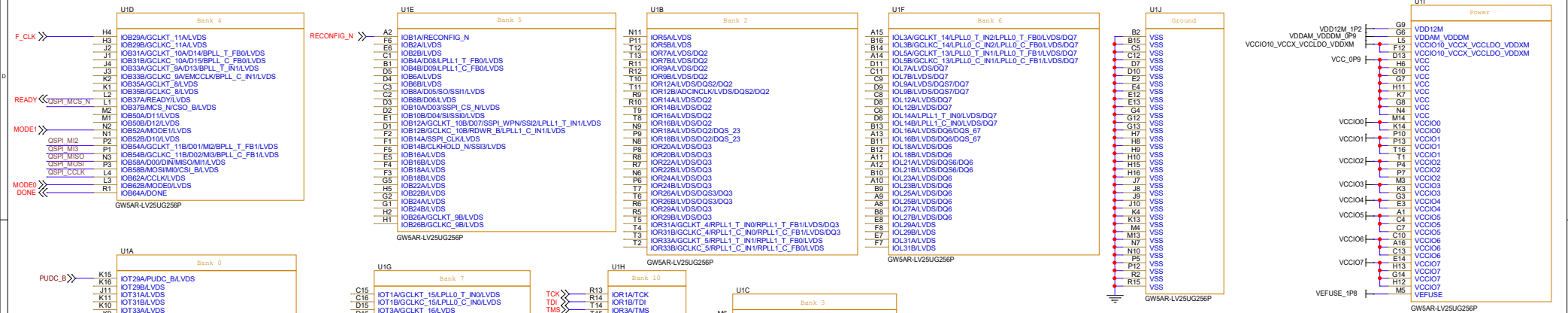
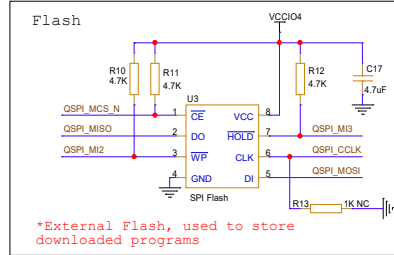
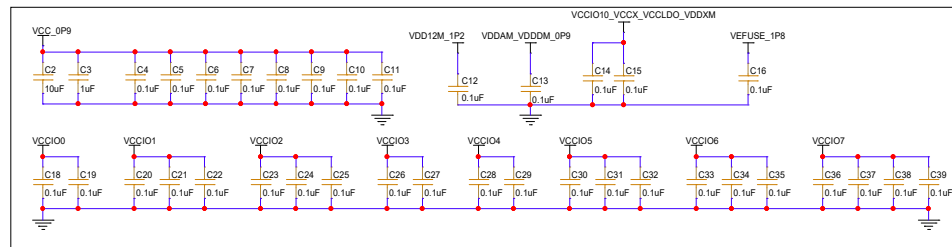
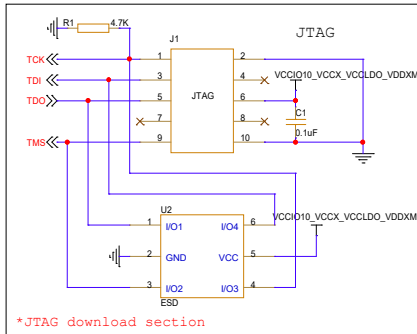
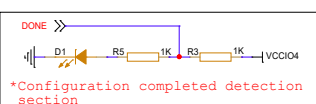
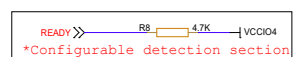
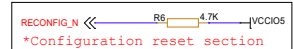
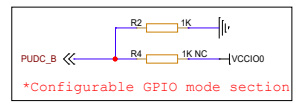


GW5AR-LV25UG256P



Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CC}	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCIO1}	I/O Bank1 supply voltage, connected to the PSRAM interface, providing PSRAM operating voltage	1.71V	1.89V
V _{CCX}	Auxiliary voltage	2.375V	3.465V
V _{CCLD0} ^[1]	Voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{EFUSE} ^[2]	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{DDAM}	Analog core power supply voltage	0.87V	1V
V _{DDDM}	Digital core power supply voltage	0.87V	1V
V _{DDIM}	Analog auxiliary voltage power supply voltage	2.375V	3.465V
V _{DD12M}	MIPI LP power supply voltage	1.14V	1.32V
PSRAM			
V _{DDP}	PSRAM power supply voltage	1.71V	1.89V
V _{DDQP}	PSRAM data bus power supply voltage	1.71V	1.89V
Note!			
^[1] The greater the V _{CCLD0} voltage, the higher the power consumption.			
^[2] When V _{EFUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			

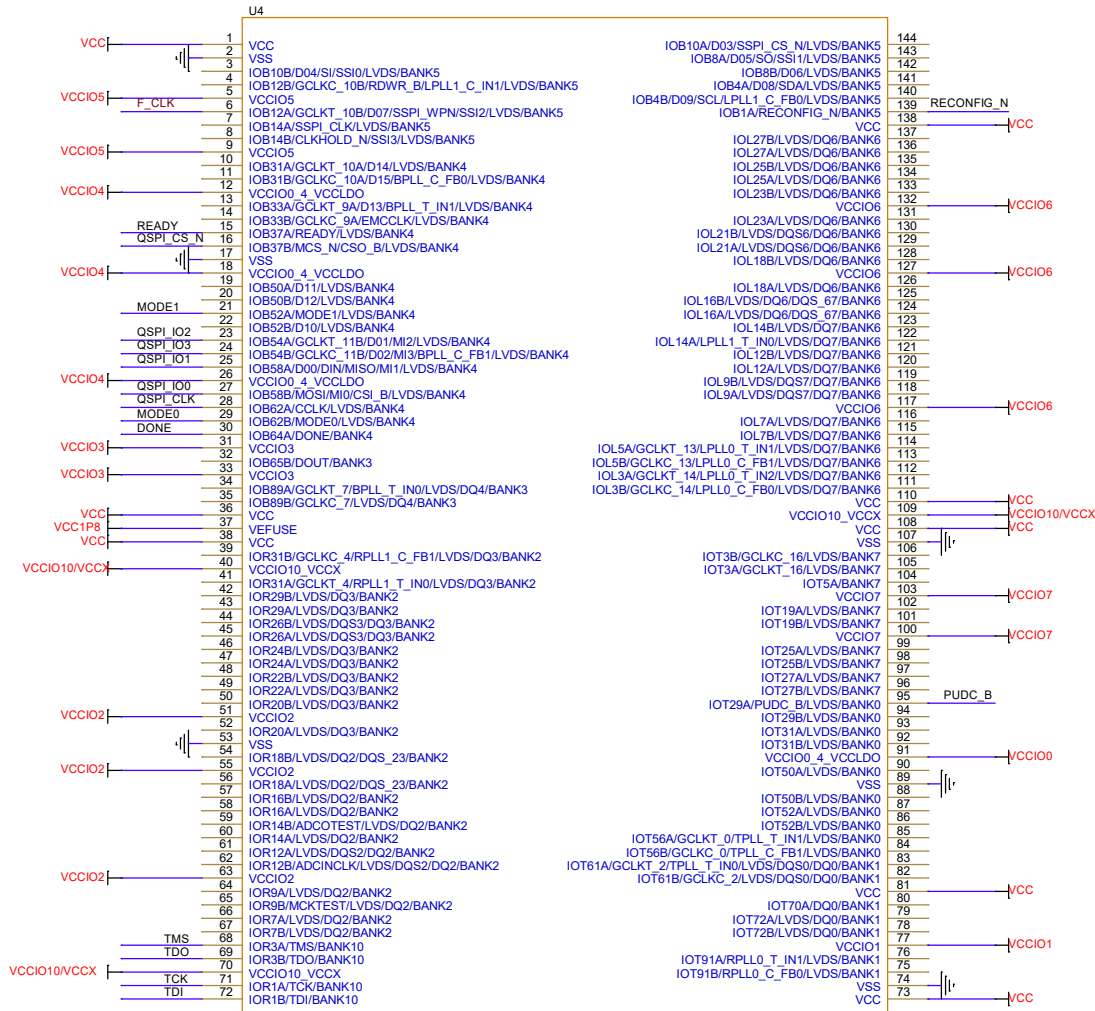


Notes:

- 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.

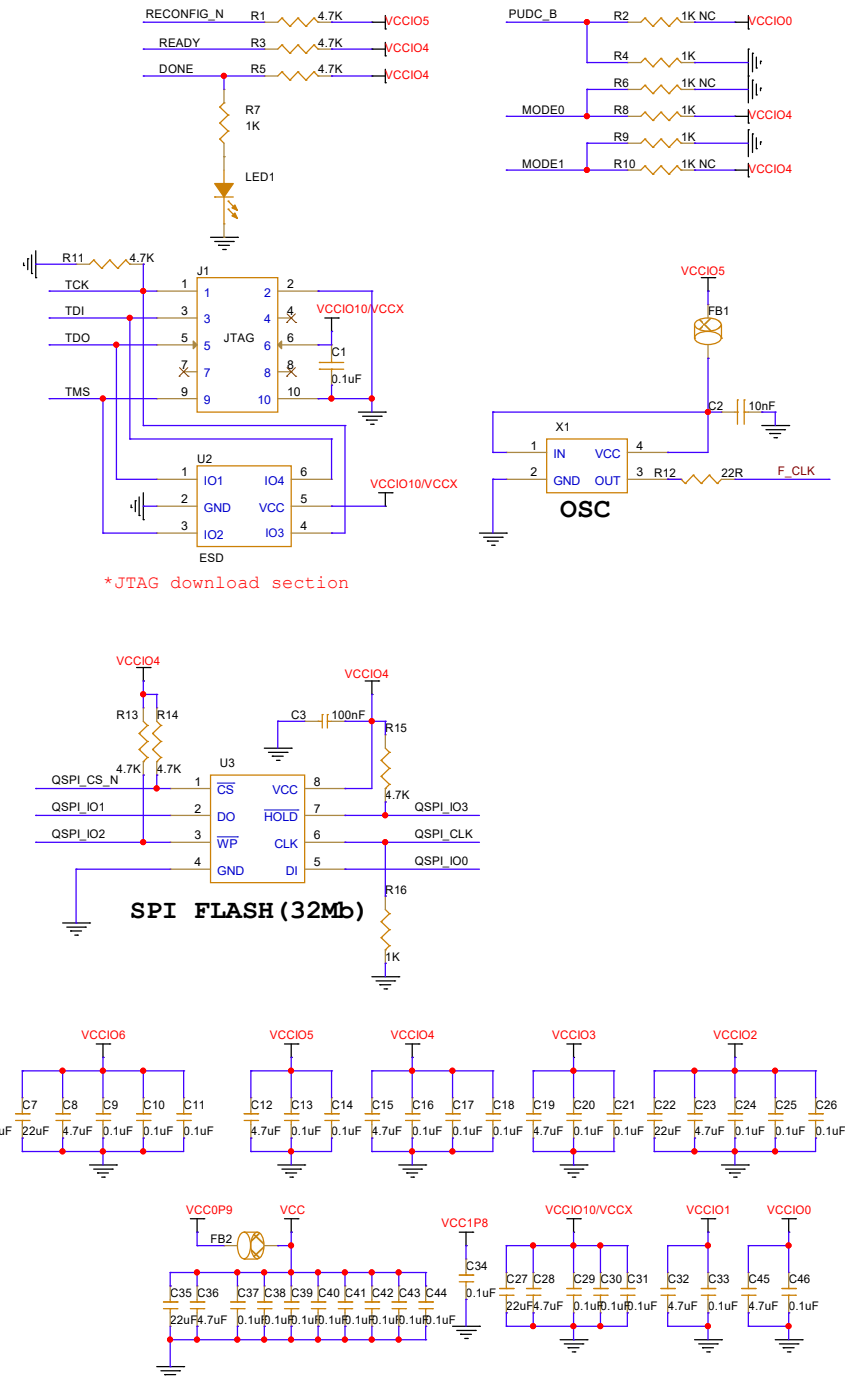
Title			
GOWIN Minimum System Diagram			
Size	Document Number	Rev	
C	GW5AR-LV25UG256P	2.4	
Date:	Wednesday, March 04, 2020	Sheet	1 of 1

GW5AR-LV25LQ144P



GW5AR-LV25LQ144P

- Notes:
- 1、It is recommended that add an ESD protection chip to the JTAG download circuit.
 - 2、The VCCX value must be set in the GOWIN EDA tool to be consistent with the actual supply voltage.
 - 3、When VEFUSE is not needed, this power supply can be connected to GND or left floating.
 - 4、PUDC_B=0: All GPIOs except PUDC_B have weak pull-up
; PUDC_B=1: All GPIOs have high impedance



File			
GOWIN Minimum System SCH			
Size	Document Number	Rev	
A3	GW5AR-LV25LQ144P	1.1	
Date:	Friday, March 27, 2026	Sheet	1 of 4